

FPGA BASED ACTIVE MAGNETIC BEARINGS CONTROLLER

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Abstract: The article discusses main problems of implementing the PID control law in the FPGA integrated circuit. Consecutive steps of discretizing and choosing the fixed-point representation of the continuous, floating-point PID algorithm are described. The FPGA controller is going to be used in the active hetero-polar magnetic bearings system consisting of two radial and one axial bearings. The results of the experimental tests of the controller are presented. The dynamic performance of the controller is better when compared with the dSPACE controller, that was used so far. The designed hardware and software, the developed implementation procedure and the experience acquired during this stage of the whole project are going to be used during the implementation of more sophisticated control laws (e.g. robust) in the FPGA for AMB controllers.

1. INTRODUCTION

Reconfigurable hardware is becoming a promising alternative to both application specific integrated circuit (ASIC) and digital signal processors (DSP) for control applications (Chen and Lin, 2002; Krach et al., 2003; Osorio-Rios et al., 2008). As a reconfigurable hardware, Field Programmable Gate Array, or FPGA, is gaining popularity. FPGA-based systems have been applied in applications ranging from signal processing, image processing, to network processors and robotics, just to name a few. The speed and size of the FPGAs are comparable with the ASICs, but FPGAs are more flexible and their design cycle is shorter because of their reconfigurability. FPGAs applications go beyond the simple implementation of digital logic. They can be used for implementations of specific architectures for speeding up some algorithm. A given algorithm, implemented into FPGA could have 100-1000 times higher performance than its implementation on a DSP or micro-processor. This is because FPGA has a natural parallel architecture for high-speed computation.

Active magnetic bearing (AMB) is a collection of electromagnets used to levitate the object via feedback control (Chiba et al., 2005). The obvious feature of the AMB is a contact-free motion control, which leads to lower rotating losses, higher speeds, elimination of lubrication system, and long life. Since an active magnetic bearing is inherently nonlinear and unstable, feedback control is indispensable to stabilize the system. A conventional PID controller is often employed as a feedback compensator and this method often yields enough stability and performance. This technique works efficiently as long as the system remains in the vicinity of the linearizing point and the uncertainties and disturbances are small. More sophisticated methods, including robust control, can improve the dynamic properties of the AMB system, especially in case of strong nonlinearities (Gosiewski and Mystkowski, 2008; Hung et al., 2003).

The view of the examined hetero-polar AMB system (Gosiewski and Mystkowski, 2008) is presented in Fig. 1. The rotor is supported by two radial and one axial magnetic bearings. The bearings include the necessary position sensors and power amplifiers. The magnetic force along each axis is generated by a pair of opposing electromagnets. The displacements of the shaft along axes are measured by five eddy-current sensors.

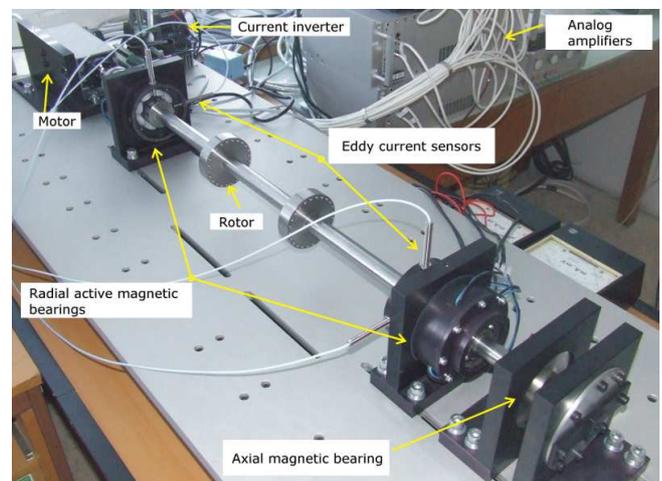


Fig. 1. View of the active magnetic bearing system

The aim of this paper is to discuss the problems of implementation of the PID algorithm for the AMB system in the FPGA. This task is a part of a bigger project concerning the design of an electromechanical flywheel energy storage. The flywheel is going to levitate in active magnetic bearing system and one of the tasks here is to design a stand-alone, FPGA-based controller. The implementation of the PID algorithm is the first stage of the design of such controller. The next will be the implementation of more sophisticated control laws, H_∞ robust, for example.

2. REQUIREMENTS

The controller should have five separate control channels to control each axis of the whole AMB system. Since the measured and control signals are analog, necessary A/D and D/A converters must be designed. The signals can change from -10 V to +10 V. The PID algorithm must be based on integer or fixed-point mathematics. This is because the FPGA used in this project has 400,000 gates and no floating point unit. Certainly, it is also possible to implement the floating point mathematics in the FPGA but this would absorb almost all its resources.

3. HARDWARE

The PID controller for the AMB system is designed with the use of two Spartan-3 LC Development Boards from Memec (2004). Spartan-3 LC board is equipped with Xilinx Spartan-3 family, XC3S400-4 PQ208CES, FPGA chip (Spartan-3, 2006). The FPGA has 400,000 gates and this is quite enough to implement three PID controller algorithms. The chip has sixteen configurable, 18-bit embedded multipliers, sixteen, 18-kbit embedded RAM blocks and two hundred and sixty four user defined input/output signals. The Spartan-3 LC board utilizes the Xilinx XCF02S Platform Flash In-System Programmable (ISP) PROM, allowing designers to store an FPGA design in non-volatile memory.



Fig. 2. Active magnetic bearings controller hardware

The board is also equipped with two push-button and four slide switches, two LEDs, one seven-segment LED display, RS232 and USB ports and two P160 connectors. FPGA can be clocked with external 50 MHz clock. There are no A/D or D/A converters on the board so we were forced to design the external converters board and power supplies for them and the whole controller. We designed and made five A/D and D/A converters boards – one for each channel of the controller. This additional boards communicate with the Spartan-3 LC board through P160 connectors and expansion boards. Each of the five boards is made of one AD976 analog to digital 16-bit converter and one two-channel AD5547 digital to analog 16-bit converter from Analog Devices (16-Bit, 100 kSPS/200 kSPS BiCMOS A/D Converters AD976/AD976A, 1999; Dual Current Output, Parallel Input, 16-/14-Bit Multiplying DACs

with 4-Quadrant Resistors AD6647/AD5557, 2004). The sampling frequency of the converters is limited to 200 kSPS.

The view of the disassembled hardware of the AMB controller is shown in Fig. 2.

4. CONTROLLER ALGORITHM IMPLEMENTATION

4.1. Difference recurrence equation

The following transfer function of the PID controller has been adopted for the AMB controller:

$$G(s) = \frac{Y(s)}{U(s)} = k_p \left(1 + \frac{1}{T_i s} + \frac{T_d s}{T_s + 1} \right), \quad (1)$$

where parameters k_p , T_i , T_d , T can change in the following ranges:

$$k_p = 0.1, \dots, 10.0, \quad T_i = 0.01, \dots, 2.0,$$

$$T_d = 0.001, \dots, 0.05, \quad T = 0.00001, \dots, 1.0.$$

For further calculations, we will assume, that $k_p = 1.5$; $T_i = 0.1$; $T_d = 0.001$; and $T = 0.0001$. Transfer function, (Eq. 1) can be transformed to the following form:

$$G(s) = \frac{Y(s)}{U(s)} = \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0}, \quad (2)$$

where: $a_2 = k_p T_i (T_d + T)$, $a_1 = k_p (T_i + T)$, $a_0 = k_p$, $b_2 = T_i T$, $b_1 = T_i$, $b_0 = 0$.

Transfer function (Eq. 2) can be also transformed to the following linear differential equation:

$$b_2 \frac{d^2 y}{dt^2} + b_1 \frac{dy}{dt} + b_0 y = a_2 \frac{d^2 u}{dt^2} + a_1 \frac{du}{dt} + a_0 u. \quad (3)$$

In order to avoid hazards that could arise in the combinatorial system, the controller algorithm should be realized as the synchronic digital system, this is the subsequent calculation steps should be taken in accordance with the clock signal. To realize this, Eq. (2) must be converted to the difference recurrence equation and discretized with the constant sample period h . The discretization process involves determining the difference representations of the subsequent differentials. Below are given the formulas for the first and second differentials of some continuous, differentiable function $x(t)$.

$$\frac{dx}{dt} \approx \frac{x(i) - x(i-1)}{h}, \quad (4)$$

$$\begin{aligned} \frac{d^2 x}{dt^2} &= \frac{\frac{dx(i)}{dt} - \frac{dx(i-1)}{dt}}{h} \\ &\approx \frac{\frac{x(i) - x(i-1)}{h} - \frac{x(i-1) - x(i-2)}{h}}{h} \\ &= \frac{x(i) - 2x(i-1) + x(i-2)}{h^2}. \end{aligned} \quad (5)$$

After using the above formulas (Eqs. 4 and 5) for the first and second differentials of functions $y(t)$ and $u(t)$, Eq. 3 can be written as follows:

$$B_2 y(i-2) + B_1 y(i-1) + B_0 y(i) = A_2 u(i-2) + A_1 u(i-1) + A_0 u(i), \quad (6)$$

where:

$$A_0 = \frac{a_2}{h^2} + \frac{a_1}{h} + a_0, \quad A_1 = -2 \frac{a_2}{h^2} - \frac{a_1}{h}, \quad A_2 = \frac{a_2}{h^2},$$

$$B_0 = \frac{b_2}{h^2} + \frac{b_1}{h} + b_0, \quad B_1 = -2 \frac{b_2}{h^2} - \frac{b_1}{h}, \quad B_2 = \frac{b_2}{h^2}.$$

In order to calculate the value of the output signal $y(i)$ for the i -th time step, Eq. 6 should be written in the following recurrence form:

$$y(i) = c_1 y(i-1) + c_2 y(i-2) + c_3 u(i) + c_4 u(i-1) + c_5 u(i-2), \quad (7)$$

where:

$$c_1 = -\frac{B_1}{B_0} = \frac{h+2T}{h+T}, \quad c_2 = -\frac{B_2}{B_0} = \frac{-T}{h+T},$$

$$c_3 = \frac{A_0}{B_0} = \frac{k_p(T_i T + T_i h + Th + T_d T_i)}{T_i(h+T)},$$

$$c_4 = \frac{A_1}{B_0} = \frac{-k_p(2T_i T + T_i h + Th + 2T_d T_i)}{T_i(h+T)},$$

$$c_5 = \frac{A_2}{B_0} = \frac{k_p(T + T_d)}{h+T}.$$

For the above given k_p, T_i, T_d, T parameters, we obtain: $c_1 = 1,952$; $c_2 = -0,952$; $c_3 = 15,780$; $c_4 = -31,489$; $c_5 = 15,708$.

Equation 7 allows us to calculate the output signal $y(i)$ on the basis of the actual values of the input signal $u(i)$ and the previous values of the output $y(i-1)$, $(i-2)$, and the input $u(i-1)$, $u(i-2)$ signals.

In case of hetero-polar AMB system the output signal $y(i)$ should be summed with the so called steady-state point signal $y_0(i)$ (Gosiewski and Mystkowski, 2008). This means that the PID controller should generate two output signals $y_1(i)$ and $y_2(i)$ (see Fig. 11) calculated in the following way:

$$y_1(i) = y_0(i) + y(i), \quad y_2(i) = y_0(i) - y(i), \quad (8)$$

where $y_0(i)$ is the steady-state point signal that is proportional to the steady-state point current i_0 .

4.2. Fixed-point representation of the signals and parameters

As was mentioned above, the controller algorithm (Eqs. 7 and 8) should be calculated using the fixed-point numbers. To do this we should choose the fixed-point representation of input signal $u(i)$, output signals $y(i)$, $y_1(i)$, $y_2(i)$ and parameters c_1, \dots, c_5 . It is especially true for output $y(i)$ and parameters c_1, \dots, c_5 as the bit-widths of signals $u(i)$

and $y_1(i)$, $y_2(i)$ are determined by the bit resolution of the A/D and D/A converters which are $w_u = 16$ and $w_y = 16$ in this case. By conducting many simulation experiments for the controller algorithms written in the floating- and fixed-point representations it was established that in order to achieve the satisfactory accuracy the following widths should be used:

$w_c = 52$, $w_{fc} = 42$ for parameters c_1, \dots, c_5 ,

$w_u = 16$, $w_{fu} = 0$ for input signal $u(i)$,

$w_y = 52$, $w_{fy} = 35$ for output signal $y(i)$,

$w_{y_1} = 16$, $w_{fy_1} = 0$ and $w_{y_2} = 16$, $w_{fy_2} = 0$

for output signals $y_1(i)$ and $y_2(i)$.

In the above given formulas the notation $w_c = 52$, $w_{fc} = 42$ means for example that the width of the fractional part of the parameter c_1 is 42 bits, the width of its integral part is 10 bits and the whole width (integral and fractional) is 52 bits.

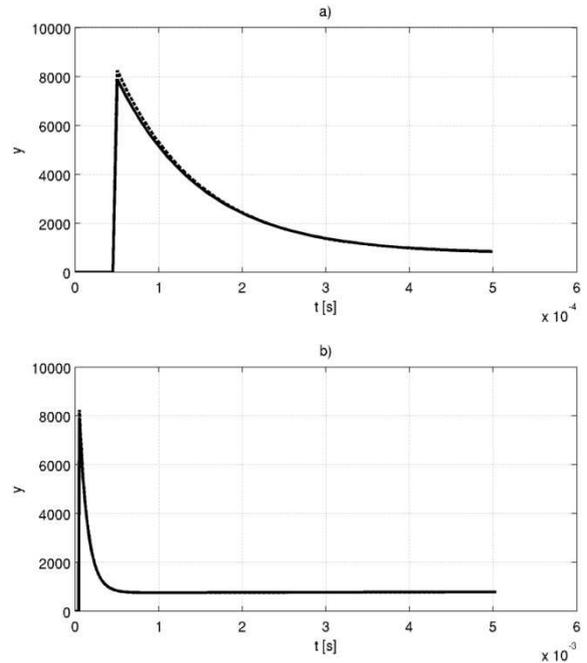


Fig. 3. Step response of the floating-point (continuous line) and the fixed-point (dashed line) representations of the PID AMB controller: a) simulation time $t = 5 \times 10^{-4}$ s, b) simulation time $t = 5 \times 10^{-3}$ s; sample period $h = 5,04 \times 10^{-6}$ s

As we can see the output signal $y(i)$ is represented with the use of 52 bits from which 35 are used to represent its fractional part, but this is true only when calculating its value according to Eq. 7. When calculating outputs y_1 and y_2 according to Eq. 8, only 16-bit integral part of y is used. This signal is obtained by cutting off the fractional part of signal y .

Input $u(i)$ and output $y(i)$, $y_1(i)$, $y_2(i)$ signals as well as controller parameters c_1, \dots, c_5 can have negative values and they are coded using the two's complement notation in which the most significant bit is the sign bit. In the hexadecimal notation that is used during coding the controller algorithm in VHDL the calculated values of the parameters are as follows:

$c_1=x"007CEDE131B8"$, $c_2=x"FFC31221ECE48"$,
 $c_3=x"03F1F140357E2"$, $c_4=x"F820B9FEC6256"$,
 $c_5=x"03ED54D03B45A"$.

Step responses of the PID controller in floating- and fixed-point representations for the above given bit-widths and various simulation times, obtained in Matlab with the use of the Fixed-Point Toolbox, are shown in Fig. 3.

4.3. 52-bit fixed-point multiplier

As we can see from Eq. 7 the calculations of the controller algorithm involve 4 summations of 104-bit wide and 5 multiplications of 52-bit wide fixed-point numbers. The multiplication can be implemented in the FPGA in various ways. The simplest is by using the basic resources, these are the so called Control Logic Blocks (CLBs). This method is also the most resource-consuming. The basic resources of the XC3S200 chip do not allow to realize even one such 52-bit operation. This is why it was decided to use the specialized 18-bit multiplication blocks embedded in the XC3S200 [8]. As we established the implementation of the 52-bit multiplication requires nine 18-bit wide embedded multiplication blocks. The whole operation is coded in VHDL using the MULT18x18 components and is placed in the mult03 entity.

To illustrate the problem the subsequent operations of the exemplary 50-bit and 40-bit wide numbers multiplication taken by 18-bit multipliers are shown in Fig. 4 (first bit is omitted as it is responsible for the sign only).

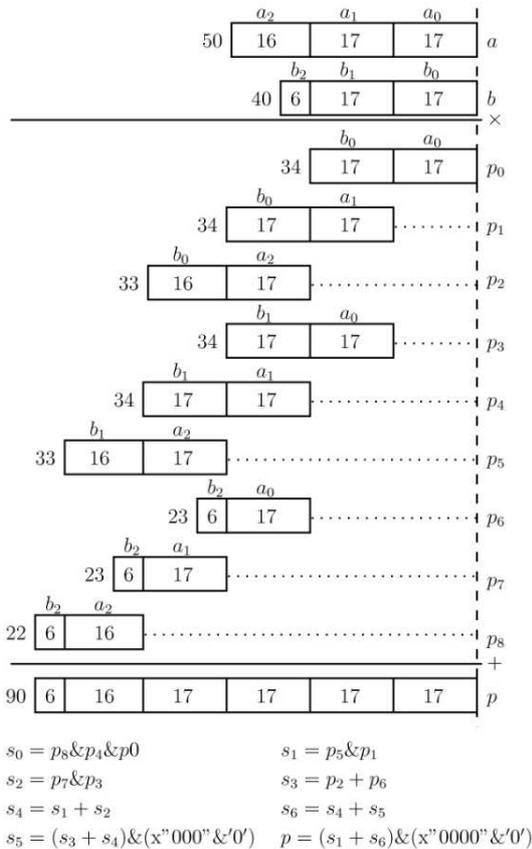


Fig. 4. Subsequent operations of the 50-bit and 40-bit wide numbers multiplication

4.4. Controller architecture

Control system for two radial and one axial AMB bearings consists of two Spartan-3 LC development boards. The first board is connected with three A/D and D/A converters boards and the second – with two A/D and D/A boards. The VHDL project for each XC3S400 FPGA consists of three PID controller cores divided into three separate channels. One of the channels is not used. That is why the whole control system for the AMBs consists of five separate PID control channels. Although each controller runs the same PID algorithm (as of Eqs. 7, 8), the parameters k_p , T_i , T_d , T can be quite different.

Schematic diagram of the designed AMB control system is shown in Fig. 5.

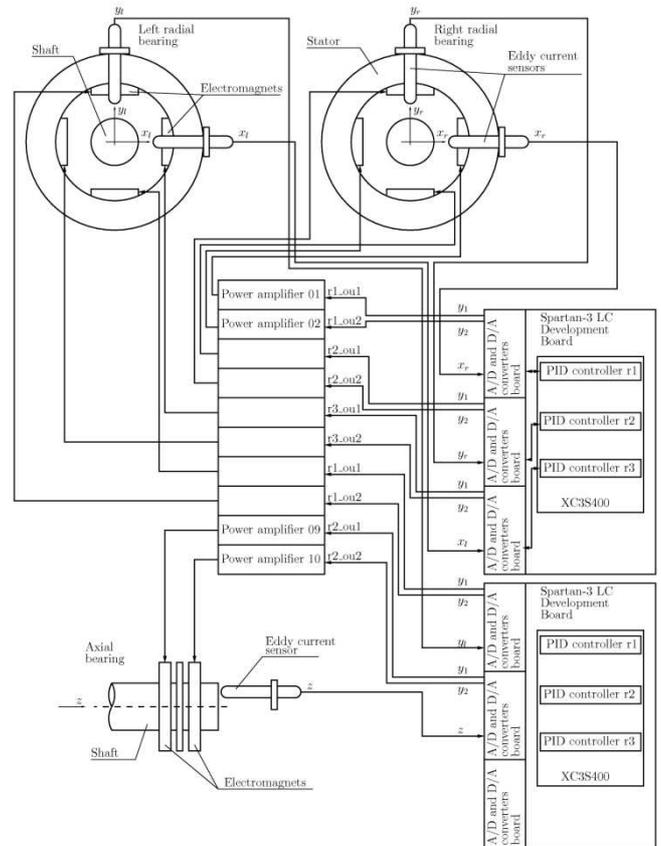


Fig. 5. Schematic diagram of the AMB control system

5. TEST RESULTS

The designed hetero-polar AMB PID controller was tested using Agilent 33220A 20MHz signals generator and Agilent 54624A oscilloscope. The resulting step responses of the controller itself (with no control loop) are shown in Figs. 6 and 7. The parameters are: $k_p = 2$; $T_i = 0,02$; $T_d = 0,001$; and $T = 1$.

The Bode plots for the first channel of the designed controller are shown in Fig. 8. The experimental characteristic has been obtained with the use of Agilent 35670A dynamic signals analyzer and compared with the simulation characteristic obtained in Matlab for the floating-point model

(Eq. 1). As we can see the magnitude plots coincide accurately. The experimental phase plot drops almost to -90° for higher frequencies what means that there is some delay in the controller. This delay is caused by the low sampling frequency of the A/D converter. Nevertheless, the dynamic properties of the designed controller for the frequency range from 10 Hz to 1 kHz that is typical for AMB control, are very good.

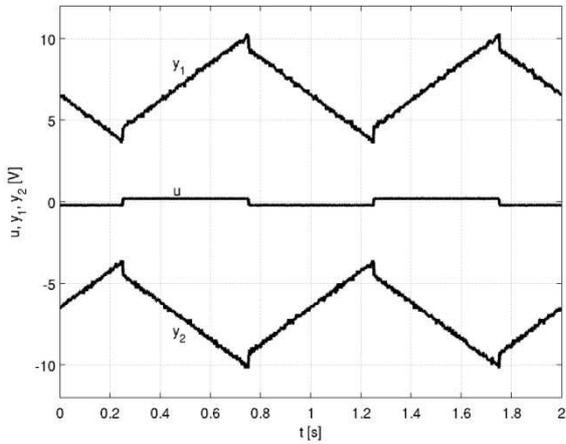


Fig. 6. Step responses y_1 and y_2 of the controller to the square input u of 1 Hz frequency and 50 mV amplitude

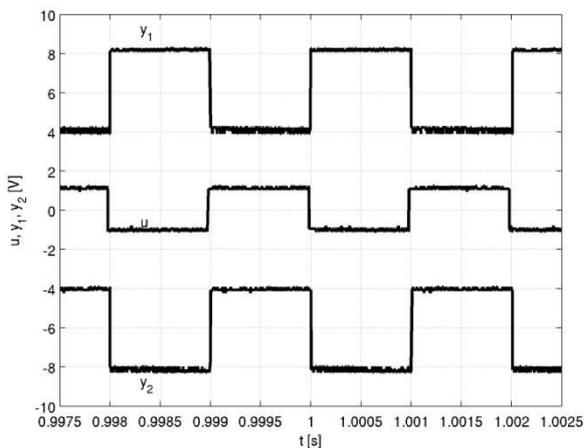


Fig. 7. Step responses y_1 and y_2 of the controller to the square input u OF 500 Hz frequency and 2 V amplitude

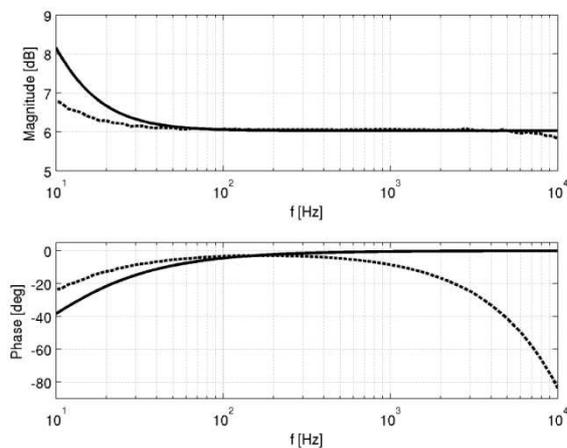


Fig. 8. Bode plots of the designed PID controller: simulation (continuous line) and experimental (dashed line)

The next step of the experimental investigations was to test the designed controller in the closed-loop AMB control system. Fig. 9 presents displacements x_l, y_l and Fig. 10 displacements x_r, y_r of the shaft in the left and the radial bearing at the moment of switching the controller on. The reference values for the displacements were as follows: $x_{lref} = -0,28V, y_{lref} = -0,25V, x_{rref} = -0,78V, y_{rref} = -0,39V$. As we can see, after a very short transient stage the controller levitates the shaft in bearings very well.

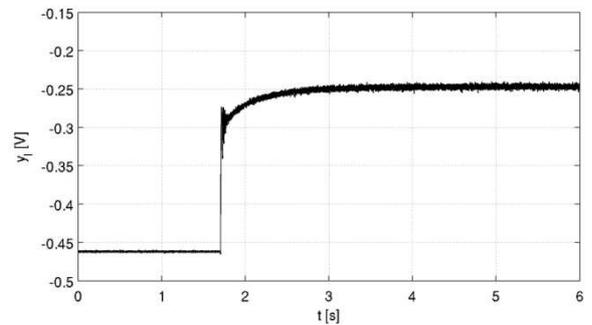
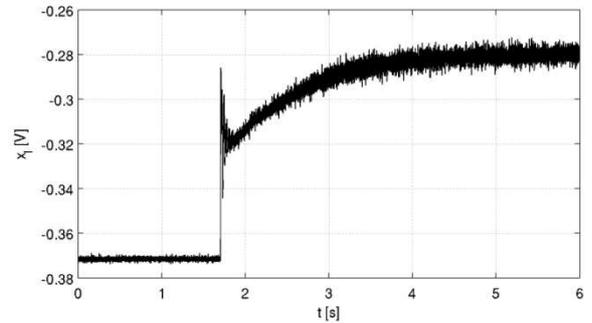


Fig. 9. Displacements x_l, y_l of the shaft in the left radial bearing

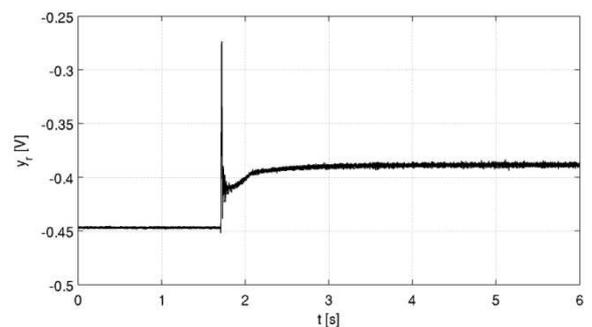
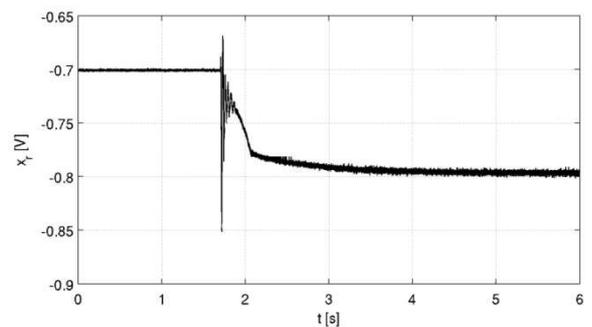


Fig. 10. Displacements x_r, y_r of the shaft in the right radial bearing

Fig. 12 presents displacements y_l and y_r of the shaft after summing output signals y_1 , y_2 of the controller with a pulse-like disturbance signal y_d as it is shown in Fig. 11. We can see a good damping of the disturbances.

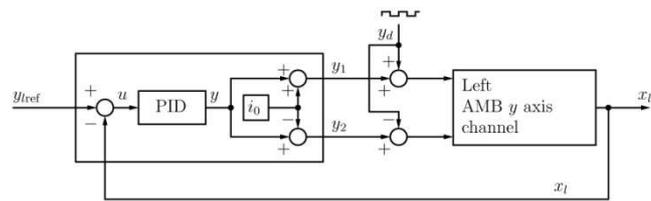


Fig. 11. Control loop of the left bearing y axis with disturbances

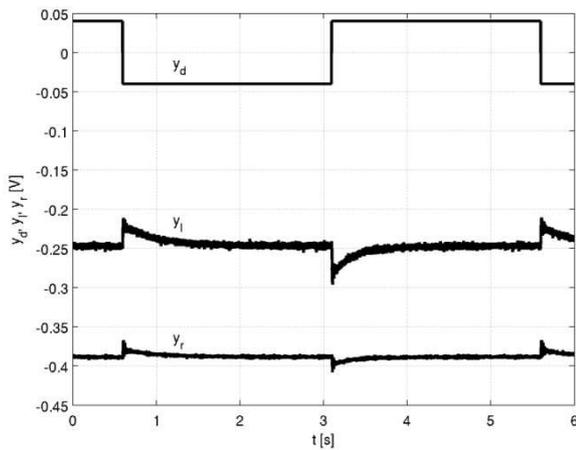


Fig. 12. Vertical displacements x_l , y_r of the shaft in both bearings with disturbance signal y_d

6. CONCLUSION

The designed hetero-polar AMB PID controller completely fulfills the preliminary requirements. It implements the PID control law in five separate control loops realized in two XC3S400 FPGAs. The FPGA resources are utilized in less than 50 percents. The dynamic performance of the controller is very good. The controller is about 20 times quicker when compared with the dSPACE controller that was used in the AMB system so far.

The main bottleneck of the controller is the low frequency of the A/D and D/A converters. The FPGA can be clocked with the very high frequency of 50 MHz and the output signal of the controllers can be calculated with this frequency too. Unfortunately this signal is updated with the frequency of 200 kHz only.

The controller can be improved by designing better A/D and D/A boards with quicker converters and by implementing better control laws.

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